CLAIMS

I claim:

1. A drive circuit for delivering high-level power to a load, the drive circuit comprising:

a high power circuit capable of being coupled to the load and delivering the high level power thereto; and

a low power circuit that controls the high power circuit, wherein the low power circuit includes

a first circuit portion that provides at least one control signal that is at least indirectly communicated to the high power circuit and that controls the delivering of the high level power by the high power circuit; and

a second circuit portion coupled to the first circuit portion,

wherein the second circuit portion is capable of disabling the first circuit portion so that the at least one control signal avoids taking on values that would result in the high power circuit delivering the high level power to the load.

2. The drive circuit of claim 1, further comprising a third circuit portion that also is coupled to the first circuit portion, wherein the third circuit portion also is capable of disabling the first circuit portion so that the at least one control signal avoids taking on values that would result in the high power circuit delivering the high level power to the load.

3. The drive circuit of claim 1, wherein the second circuit portion includes a safety relay circuit that is coupled to a power terminal of the first circuit portion, and wherein the safety relay circuit decouples the power terminal of the first circuit from a power supply in order to disable the first circuit portion.

4. The drive circuit of claim 1, wherein the second circuit portion includes a safety relay circuit that is coupled to a pull-up resistor of the first circuit portion, and wherein the safety relay circuit disables the first circuit portion by at least one of coupling the pull-up resistor to ground and decoupling the pull-up resistor from a power supply.

5. The drive circuit of claim 4, wherein the safety relay circuit additionally is coupled to a power terminal of the first circuit portion, and wherein the safety relay circuit couples the power terminal of the first circuit portion to ground in order to further disable the first circuit portion.

6. The drive circuit of claim 4, wherein the safety relay circuit includes a coil, a normally-open contact, and a normally-closed contact, wherein the contacts are physically coupled so that only one of the contacts can be closed at any given time, and wherein the safety relay circuit disables the first circuit portion when power is provided to the coil.

7. The drive circuit of claim 1, wherein the second circuit includes a component that is coupled to an override port of the first circuit, and wherein the second circuit disables the first circuit by providing a first signal to the override port of the first circuit.

8. The drive circuit of claim 7, wherein the second circuit includes a hardware switch that is capable of being switched between first and second states, and wherein when the switch is switched in the first state, the second circuit provides the first signal to the override port of the first circuit.

9. The drive circuit of claim 8, wherein the second circuit further includes a NOR gate having first and second input terminals, wherein the NOR gate receives a second signal from the hardware switch and a third signal from the first circuit at the first and second input terminals, and wherein the NOR gate outputs a fourth signal that is one of equal to or functionally related to the first signal.

10. The drive circuit of claim 8, wherein the high power circuit includes at least one coil that outputs a signal indicative of a current delivered by the high power circuit to the load, and wherein a determination is made regarding whether the signal indicative of the current is proper when the switch is switched in the first state.

11. The drive circuit of claim 1, wherein the first circuit includes a microprocessor, an inverter circuit, and a buffer circuit.

12. The drive circuit of claim 11 wherein, when the first circuit is not disabled, the microprocessor outputs a plurality of preliminary signals to the inverter circuit, the inverter circuit converts the plurality of preliminary signals into a plurality of modified signals, and the buffer circuit provides the at least one control signal in response to the plurality of modified signals, and each of the preliminary signals, the modified signals, and the at least one control signal is a pulse width modulated (PWM) signal.

13. The drive circuit of claim 11,

wherein the inverter circuit has open collector output terminals that are coupled to the buffer circuit,

wherein the second circuit portion includes a safety relay circuit that is coupled to a pull-up resistor that is coupled between the safety relay circuit and both one of the open collector output terminals and a corresponding input terminal of the buffer circuit, and

wherein the safety relay circuit at least one of decouples the pull-up resistor from a power supply and couples the pull-up resistor to a ground in order to disable the first circuit portion.

14. The drive circuit of claim 13,

wherein the safety relay circuit also is coupled to an additional pull-up resistor that is coupled to a third circuit portion that is coupled to an enable input of the buffer circuit, and wherein the safety relay circuit at least one of decouples the additional pull-up resistor from the power supply and couples the additional pull-up resistor to the ground in order to further disable the first circuit portion by disabling the buffer circuit.

15. The drive circuit of claim 1, wherein the high power circuit includes a plurality of high power transistor devices that are light-actuated and a plurality of photodiodes receive the at least one control signal from the lower power circuit, and wherein the high power transistor devices are electrically isolated from the photodiodes.

16. The drive circuit of claim 1, wherein the second circuit portion includes an isolation device that is capable of communicating a signal provided from an additional device to the first circuit portion.

17. The drive circuit of claim 16, wherein the isolation device includes one of a DC-to-DC converter and an optical isolator.

18. A high power drive circuit for delivering power to a motor, the high power drive circuit comprising:

first means for delivering high power to the motor;

second means for generating low power control signals for the first means; and

third means for disabling the second means so that the low power control signals take on values that would tend to cause the first means to stop delivering the high power to the motor.

19. The high power drive circuit of claim 18, wherein the third means includes at least first and second inputs that can be independently switched to cause the third means to disable the second means.

20. A method of stopping a high power load from operating, wherein the high power load receives power from a drive circuit having a high power drive section and a low power logic section, and wherein the low power logic section provides a control signal to the high power drive section and the high power drive section during normal operation provides the power to the high power load in response to the control signal, the method comprising:

receiving a command to stop the high power load from operating; and

switching a status of at least a first component of the low power logic section in response to the command, wherein the switching of the status affects one of the first component and a second component of the low power logic section so that the control signal provided by the low power logic section takes on a value that would tend to cause the high power drive section to cease providing the power to the high power load; and

ceasing to provide the power to the high power load in response to the control signal taking on the value.

21. The method of claim 20, wherein the switching of the status includes at least one of the following:

decoupling a power supply from a power supply terminal of a buffer circuit of the low power logic section;

decoupling a power supply from a pull-up resistor of the low power logic section, wherein the pull-up resistor is also coupled to both an output of an inverter circuit having an open collector output and an input of the buffer circuit;

coupling the pull-up resistor of the low power logic section to a ground; and

providing an intermediate signal to an enable/disable port of the buffer circuit such that the buffer circuit becomes disabled.

22. The method of claim 20, wherein the command is provided by way of at least one of an actuation of a component in a safety relay circuit, an actuation of a hardware switch, and a sending of a signal from a control component within the low power logic section.

23. A drive circuit for delivering high-level power to a load, the drive circuit comprising:

a high power circuit capable of being coupled to the load and delivering the high level power thereto; and

a low power circuit that controls the high power circuit, wherein the low power circuit includes a first circuit portion that provides at least one control signal that is at least indirectly communicated to the high power circuit and that controls the delivering of the high level power by the high power circuit;

wherein the first circuit portion is at least one of coupled to, and adapted to be coupled to, a second circuit portion that is capable of providing to the first circuit portion at least one additional signal causing the first circuit portion to become disabled so that the at least one control signal avoids taking on values that would result in the high power circuit delivering the high level power to the load.